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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/726,114	11/30/2000	Shigetaka Kumashiro	Q61995	9701

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EXAMINER	
CRAIG, DWIN M	
ART UNIT	**PAPER NUMBER**
2123	4

DATE MAILED: 07/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,114	KUMASHIRO, SHIGETAKA	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11-30-2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,10,11,15,19 and 20* is/are rejected.

7)☒ Claim(s) *3-5, 7-9, 12-14 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been presented for Examination. Claims 1, 2, 6, 10, 11, 15, 19 and 20 are rejected. Claims 3-5, 7-9, 12-14 and 16-18 are objected to.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Independent **Claims 1, 10, 19 and 20** and dependent **Claims 6 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bittner et al. U.S. Patent 6,314,390** in view of **Nobe et al. U.S. Patent 5,296,723.**

3.1 As regards independent **Claims 1, 10, 19 and 20** the *Bittner et al.* reference discloses MOSFET models used in a computer simulation **(Figures 1 & 2),** using the BSIM3v3.2 MOSFET model **(Col. 4 Lines 63-67, Col. 5 Lines 1-14).**

However the *Bittner et al.* reference does not expressly disclose a model of a MOSFET including diodes connected in parallel to the source and drain of the MOSFET.

The *Nobe et al.* reference discloses a model of a MOSFET including diodes connected in parallel to the source and drain of the MOSFET **(Figure 5).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the modeling methods of the *Bittner et al.* reference with the circuit configuration of the *Nobe et al.* reference because, by configuring parallel diodes to the source and drain of a MOSFET a lower distortion amplifier can be designed ***(Nobe et al. Col. 2 Lines 40-48).***

3.2 As regards dependent **Claims 6 and 15** the *Bittner et al.* reference does not expressly disclose anodes tied to gates of MOSFETS.

The *Nobe et al.* reference discloses diodes tied to gates of MOSFETS **(Figure 4).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the modeling methods of the *Bittner et al.* reference with the circuit configuration of the *Nobe et al.* reference because, by configuring parallel diodes to the source and drain of a MOSFET a lower distortion amplifier can be designed ***(Nobe et al. Col. 2 Lines 40-48).***

4. Dependent **Claims 2 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bittner et al. U.S. Patent 6,314,390** in view of **Nobe et al. U.S. Patent 5,296,723** and in further view of "**Fundamentals of Modern VLSI Devices**" by **Yuan Taur and Tak H. Ning** *hereafter referred to as the Taur et al. reference.*

4.1 As regards independent **Claims 1 and 10** see section **3.1** above.

4.2 As regards dependent **Claims 2 and 11** the *Bittner et al.* reference does not expressly disclose insulating film that is thinner than 2nm.

The *Taur et al.* reference discloses insulating film that is thinner than 2nm **(page 97).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the MOSFET modeling methods of the *Bittner et al.* reference with the because an artisan of ordinary skill would be aware of the tunneling effects as disclosed in the *Taur et al.* reference and would have been motivated to use those disclosed methods in the simulation of a MOSFET gate that had an insulating film of less than 2nm in order to have a more accurate simulation.

Allowable Subject Matter

5. **Claims 3-5, 7-9, 12-14 and 16-18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- U.S. Patent 5,845,275 discloses a method of modeling transistor performance using diodes and fuzzy logic.
- "Modeling of direct tunneling gate current in ultra-thin gate oxide MOSFETs: a comparison between simulators" by E. Cassan, S. Galdin, P.Dollfus and P. Hesto, discloses methods of modeling thin gate MOSFETS.

6.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER